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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/632,543	08/04/2000	Rajendra K. Talluri	TI-28919	1760

23494 7590 08/04/2008
TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
NGUYEN, LUONG TRUNG	
ART UNIT	PAPER NUMBER
2622	

NOTIFICATION DATE	DELIVERY MODE
08/04/2008	ELECTRONIC

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte RAJENDRA K. TALLURI, CHING-YU HUNG,
KLAUS ILLGNER, YOUNGJUN YOO,
JIE LIANG, MANDY TSAI,
KIYOSHI TSUNODA and SHINRI INAMORI

Appeal 2008-0825
Application 09/632,543[1]
Technology Center 2600

Decided: July 31, 2008

Before ROBERT E. NAPPI, MARC S. HOFF,
and KEVIN TURNER, *Administrative Patent Judges*.

HOFF, *Administrative Patent Judge*.

DECISION ON APPEAL

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[1] Application filed August 4, 2000. The real party in interest is Texas Instruments Incorporated.

STATEMENT OF CASE

Appellants appeal under 35 U.S.C. § 134 from a Final Rejection of claims 1 and 3-6.[2] We have jurisdiction under 35 U.S.C. § 6(b).

We affirm-in-part.

Appellants' invention relates to a digital still camera having dual processors, an image coprocessor, a burst mode compression/decompression engine, and a programmable preview engine (Spec. 2).

Claims 1 and 4 are exemplary:

1. An integrated circuit for a digital still camera, comprising:

(a) a first programmable processor programmed to run control functions, said first processor coupled to a user interface, a controller for memory, and a controller for image acquisition;

(b) a second programmable processor programmed to run image processing and compression functions, said second processor coupled to said first processor; and

(c) a third processor coupled to said second processor, said third processor including at least four parallel multiply and accumulate units.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Fukuoka	Re. 36, 338	Oct. 12, 1999
Duncan	US 6,597,394	Jul. 22, 2003
Safai	US 6,642,956	Nov. 4, 2003
Mizutani	US 6,674,464	Jan. 6, 2004

[2] Claim 2 has been canceled.

Claim 1 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Duncan.

Claim 4 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Fukuoka.

Claim 3 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Safai in view of Mizutani.

Claim 5 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Duncan in view of Fukuoka.

Claim 6 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Duncan in view of Safai and Mizutani.

Appellants contend that Duncan does not anticipate claim 1 because Duncan lacks four parallel multiply and accumulate units; that the person of ordinary skill in the art would not have been motivated to combine Safai and Mizutani to meet claim 3; and that Fukuoka does not anticipate claim 4 because Fukuoka's "second processor" is not programmable.

Rather than repeat the arguments of Appellants or the Examiner, we make reference to the Brief (filed June 20, 2006[3]) and the Answer (mailed September 7, 2006) for their respective details.

ISSUE

There are three principal issues in the appeal before us.

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[3] Appellants filed a Supplemental Brief on November 1, 2006, responsive to a Notification of Non-Compliant Appeal Brief. However, the Supplemental Brief is not substantively different from the originally filed Brief, and the Examiner made no response to the Supplemental Brief.

The first issue is whether the Examiner erred in holding that Duncan teaches elements corresponding to the four parallel multiply and accumulate units recited in claim 1.

The second issue is whether the Examiner erred in holding that Safai in combination with Mizutani teach an image compression unit separate from the second processor, arranged to compress acquired images, as recited in claim 3.

The third issue is whether the Examiner erred in holding that Fukuoka teaches a second programmable processor programmed to run image processing and compression functions, as recited in claim 4.

FINDINGS OF FACT

The following Findings of Fact (FF) are shown by a preponderance of the evidence.

The Invention

1. According to Appellants, they have invented a digital still camera having dual processors, an image coprocessor, a burst mode compression/decompression engine, and a programmable preview engine (Spec. 2).

Duncan

2. Duncan teaches a programmable image transform processor having programmable addressing and arithmetic blocks (col. 2, ll. 44-45).

3. Duncan's image transform processor teaches a plurality of multipliers (630-633), each having a latch (640-643) associated therewith (Fig. 6A; col. 15, ll. 15-48).

Fukuoka

4. Fukuoka teaches an electronic still camera in which image and sound interlaced and recorded to a recording medium can be regenerated from the recording medium (col. 1, ll. 60-63).

5. Fukuoka teaches that corrected image data are transmitted to an image data compressing-extending circuit 7 as an image data encoding means and an image data decoding means, which "encodes the image data" (col. 4, ll. 30-34).

Safai

6. Safai teaches a digital image processor for use in a digital camera (col. 2, l. 21).

Mizutani

7. Mizutani teaches imaging apparatus for performing signal processing depending on operational mode (col. 1, ll. 8-10).

8. Mizutani includes a separate unit (JPEG unit 29, Figs. 2, 3; col. 6, ll. 25-30) that performs image compression *and* decompression.

PRINCIPLES OF LAW

Anticipation is established when a single prior art reference discloses expressly or under the principles of inherency each and every limitation of the claimed invention. *Atlas Powder Co. v. IRECO, Inc.*, 190 F.3d 1342, 1347 (Fed. Cir. 1999); *In re Paulsen*, 30 F.3d 1475, 1478-79 (Fed. Cir. 1994).

"Section 103 forbids issuance of a patent when 'the differences between the subject matter sought to be patented and the prior art are such

that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.'" *KSR Int'l Co. v. Teleflex Inc.*, 127 S.Ct. 1727, 1734, (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, (3) the level of skill in the art, and (4) where in evidence, so-called secondary considerations. *Graham v. John Deere Co.*, 383 U.S. 1, 17-18, (1966). *See also KSR*, 127 S. Ct. at 1734 ("While the sequence of these questions might be reordered in any particular case, the [*Graham*] factors continue to define the inquiry that controls.")

ANALYSIS

Claim 1

Appellants argue that Duncan does not teach four parallel multiply and accumulate units, as required by the claim, because "there is no accumulation for each multiplier" (Br. 4) and Duncan teaches a single accumulator (*Id.*).

We find Appellants' argument unpersuasive. We agree with the Examiner that a latch is used for "holding (accumulating or storing) data" (Ans. 7). Therefore, the multipliers 630-633 and latches 640-643 (FF 3) of Duncan may fairly be construed to meet the required multiply and accumulate units.

We therefore do not find error in the Examiner's rejection of claim 1 under 35 U.S.C. § 102(e).

Claim 3

Appellants argue that motivation to combine Safai and Mizutani is lacking. Appellants assert that because the processor in Safai equated by the Examiner with the "second processor" (310) does image compression, there would have been no need for the skilled artisan to look to Mizutani for a separate image compression unit, and thus no motivation to combine Safai with Mizutani (Br. 5). Appellants further argue that Mizutani's image compression unit (JPEG unit 29) does not "act on the acquired image," as the claim requires, because the JPEG unit is "applied after input processing 21 and memory controller 22" (Br. 5).

We agree with the Examiner, however, that Appellants' first argument is not persuasive, because Safai's second processor (digital image processor 310, Fig. 3; col. 5, ll. 45-58) lacks image *decompression* functionality (Ans. 8). Absent some modification, therefore, the two processors in Safai could not perform the functions required by the claim. Mizutani does teach a separate unit that performs image compression *and* decompression (FF 8). Appellants' second argument is similarly unpersuasive, because claim 3 does not require the image compression unit to be *directly* connected to any image acquiring element. The claim merely requires that the compression unit be "arranged to compress acquired images." JPEG unit 29 of Mizutani functions to compress acquired images (*Id.*).

Because we find that the combination of Safai and Mizutani fairly suggests the claimed invention, we do not find error in the Examiner's rejection of claim 3 under 35 U.S.C. § 103.

Claim 4

Appellants argue that Fukuoka does not anticipate claim 4 because Fukuoka's image data compressing-extending circuit 7 does not meet the limitation of a "programmable processor" (Br. 5). In the Examiner's view, because circuit 7 receives control operation from CPU 11, it "is programmable in order to receive control operation from CPU 11" (Ans. 8).

We disagree with the Examiner that any particular element is necessarily programmable merely because it is controlled by, or receives control information or signals from, another element that *is* programmable (in Fukuoka, CPU 11). A microprocessor or microcontroller may control any number of non-programmable devices (e.g., indicator lights). In our view, a programmable device is one whose program is changeable by the operator, either in advance or in real time. The Examiner has not pointed to any teaching in Fukuoka to which presents sufficient evidence to support a finding that the image data compressing-extending circuit 7 has an alterable program. We are unable to find any description of the circuit beyond that it "encodes the image data" (FF 5). Without more, the Examiner has not established that Fukuoka's compressing-extending circuit reads on the claimed "second programmable processor."

Because the Examiner has not established that every element of claim 4 is present in Fukuoka, we find error in the Examiner's rejection of claim 4 under 35 U.S.C. § 102.

Claim 5

With respect to the patentability of this claim, Appellants "rely upon the patentability of parent claim 1" (Br. 5). Therefore, because we affirm the rejection of claim 1, *supra*, we also affirm the rejection of claim 5, for the same reasons.

Claim 6

With respect to the patentability of this claim, Appellants "rely on the patentability of claim 1" (Br. 5). Therefore, because we affirm the rejection of claim 1, *supra*, we also affirm the rejection of claim 6, for the same reasons.

CONCLUSION OF LAW

We conclude that Appellants have not shown that the Examiner erred in rejecting claims 1, 3, 5, and 6. Claims 1, 3, 5, and 6 are not patentable.

We conclude that Appellants have shown that the Examiner erred in rejecting claim 4. On the record before us, claim 4 has not been shown to be unpatentable.

DECISION

The Examiner's rejection of claims 1, 3, 5, and 6 is affirmed. The Examiner's rejection of claim 4 is reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

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TEXAS INSTRUMENTS INCORPORATED
P. O. BOX 655474, M/S 3999
DALLAS, TX 75265